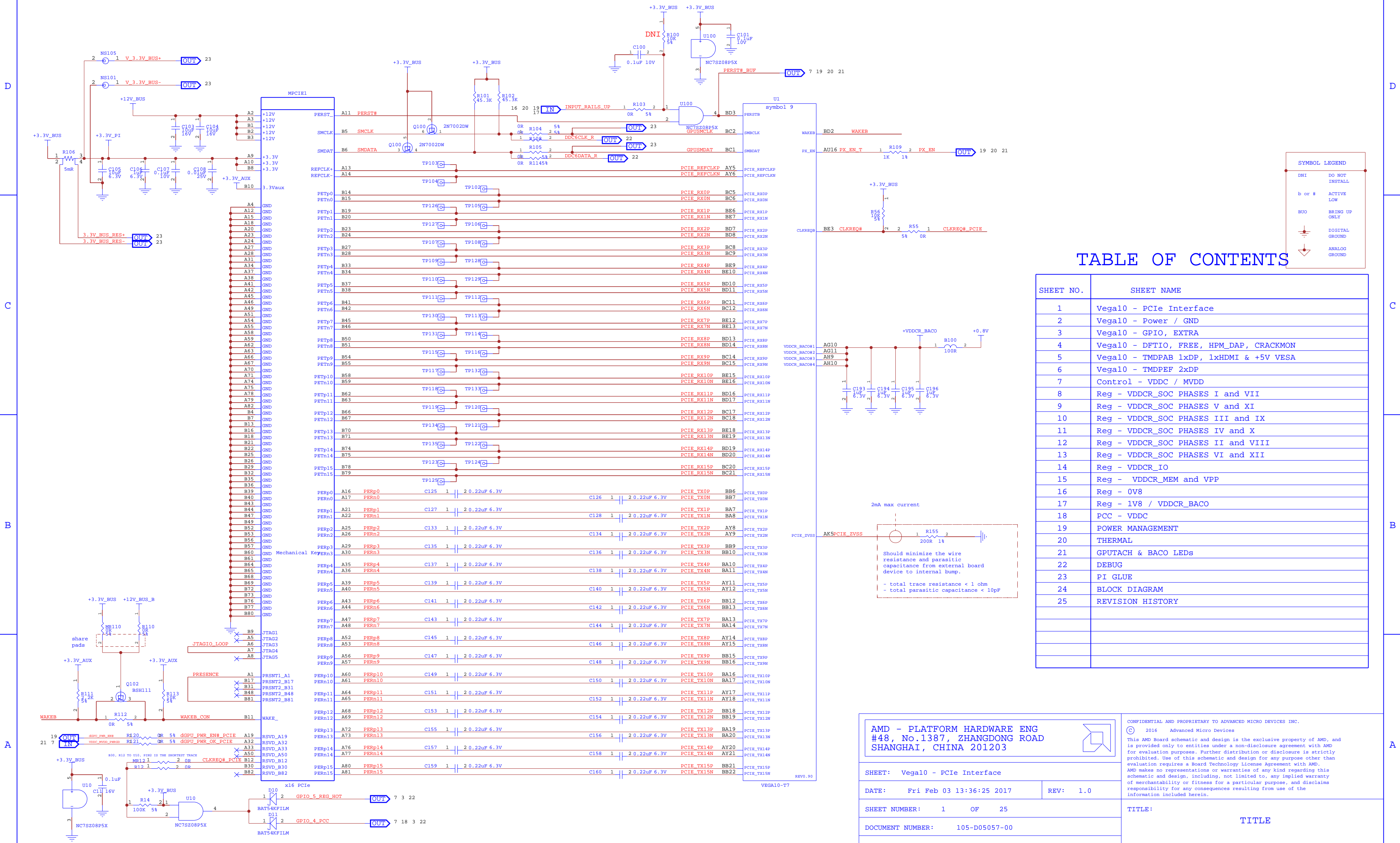
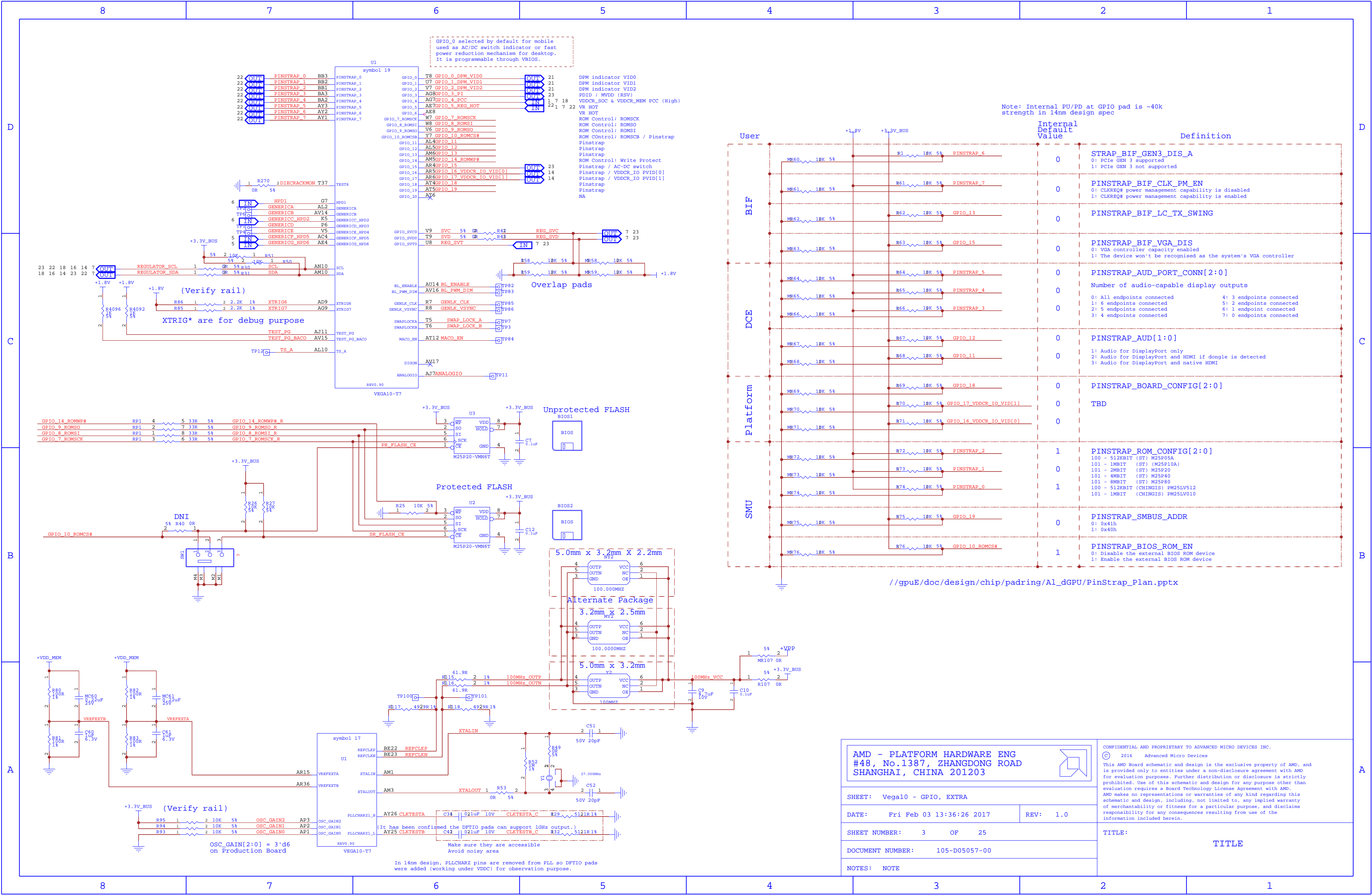


1. Vega10 PCIe Edge Connector





AMD - PLATFORM HARDWARE ENG
#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Vega10 - GPIO, EXTRA

DATE: Fri Feb 03 13:36:26 2017

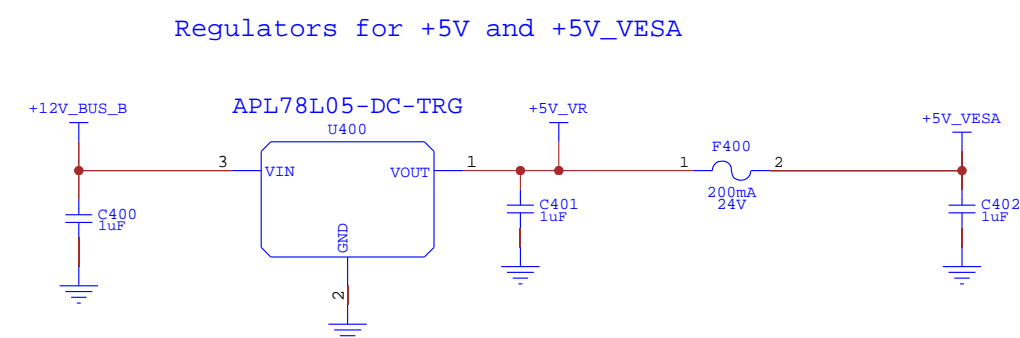
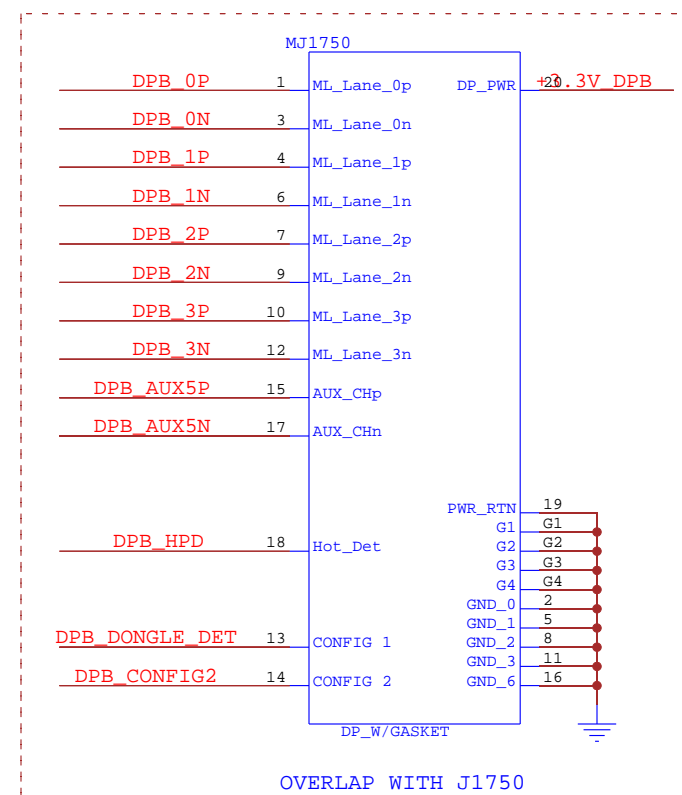
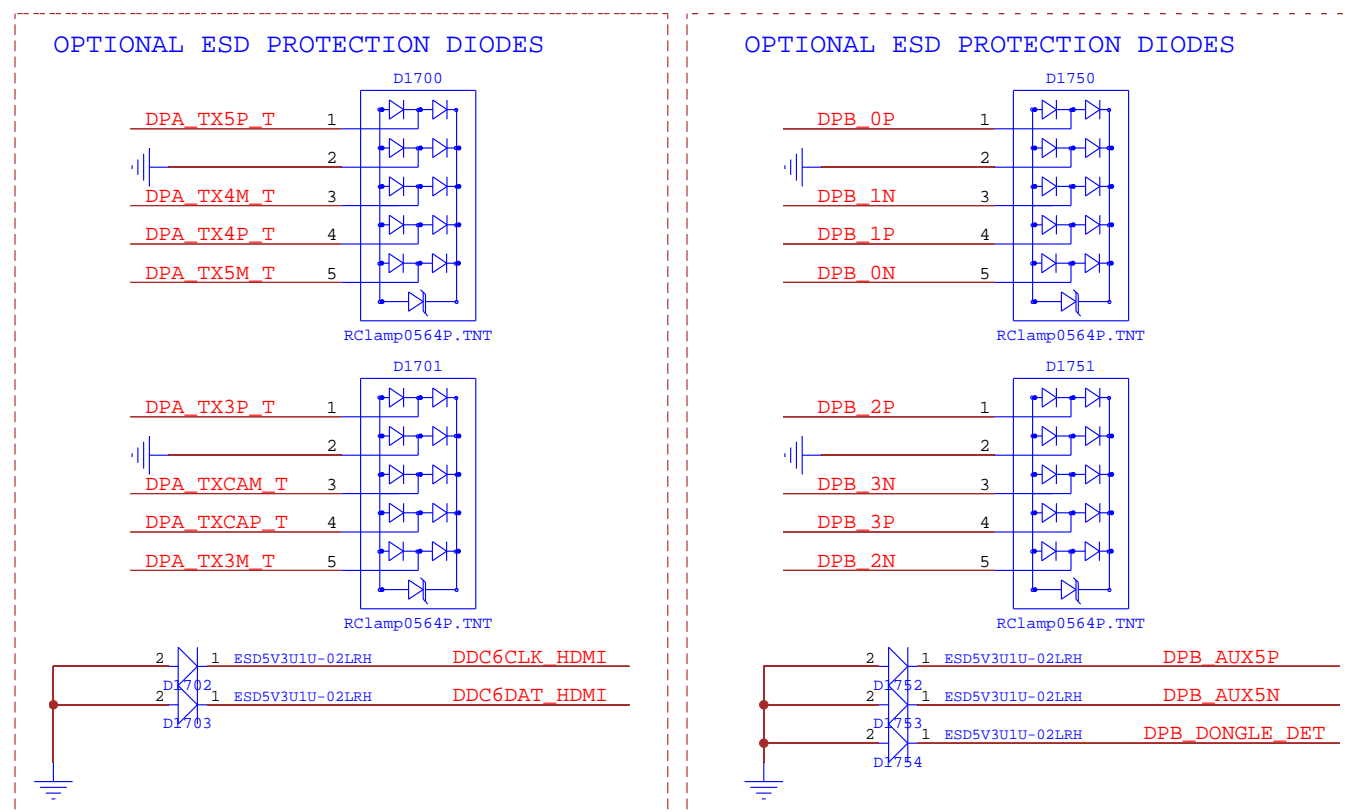
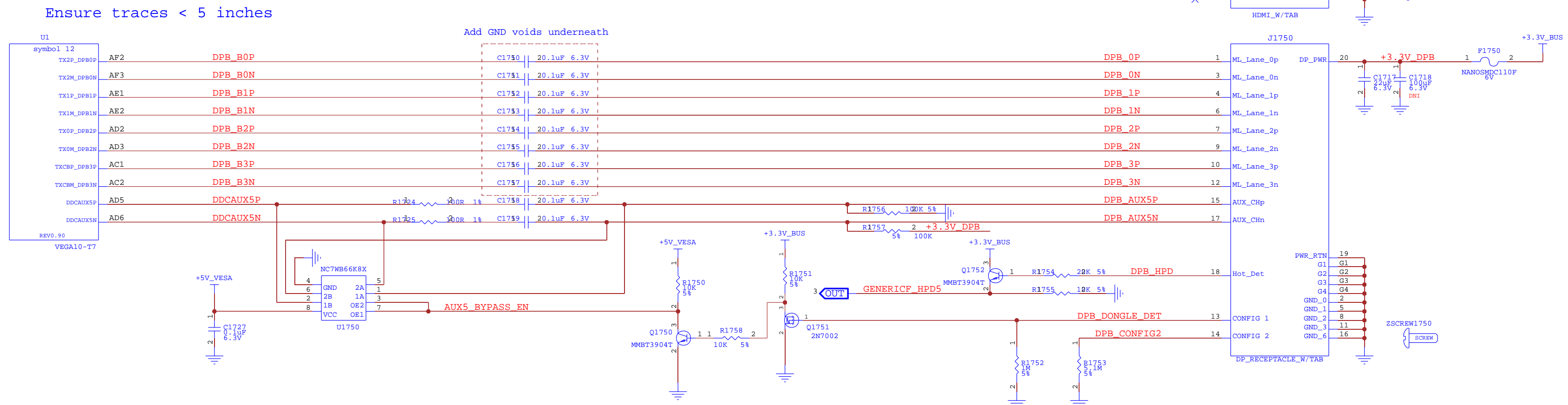
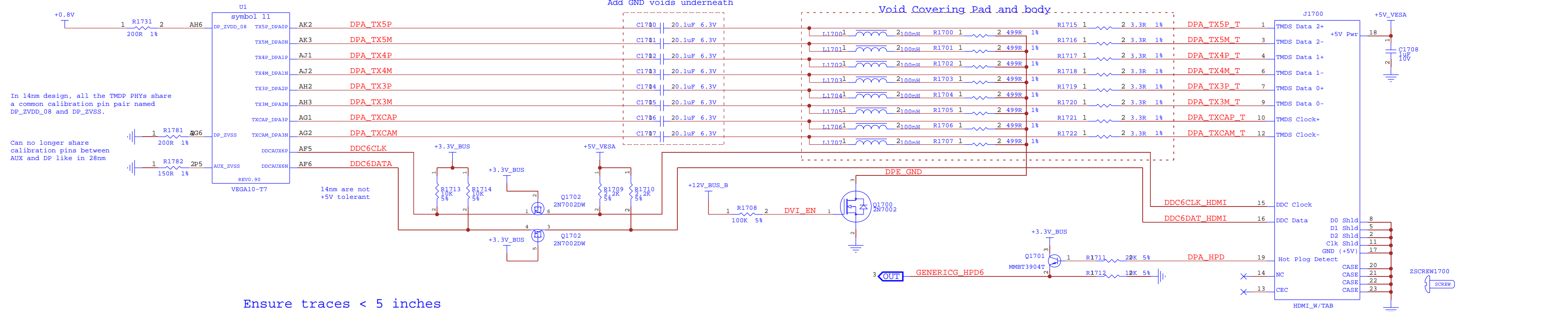
SHEET NUMBER: 3 OF 25

DOCUMENT NUMBER: 105-D05057-00

NOTES: NOTE

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SHEET: Vega10 - TMDPAB 1xDP, 1xHDMI & +5V VESA

DATE: Fri Feb 03 13:36:26 2017 REV: 1.0

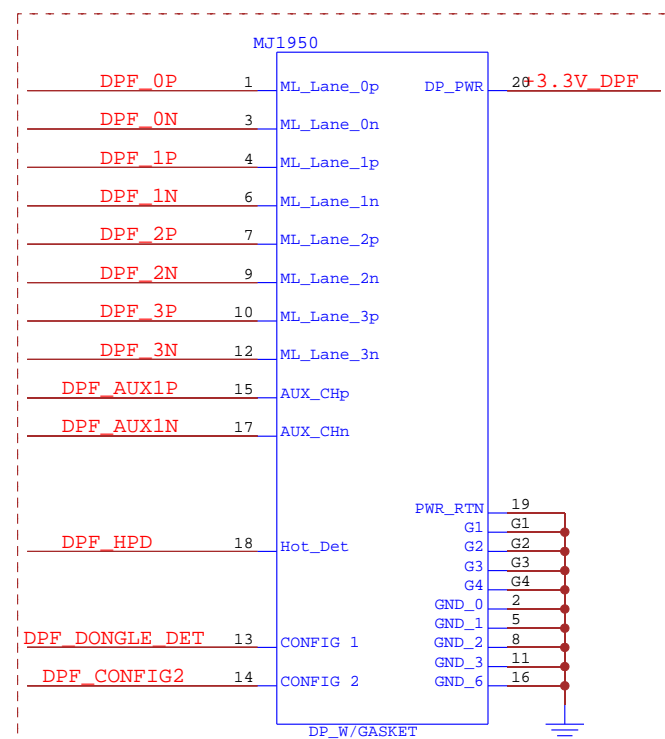
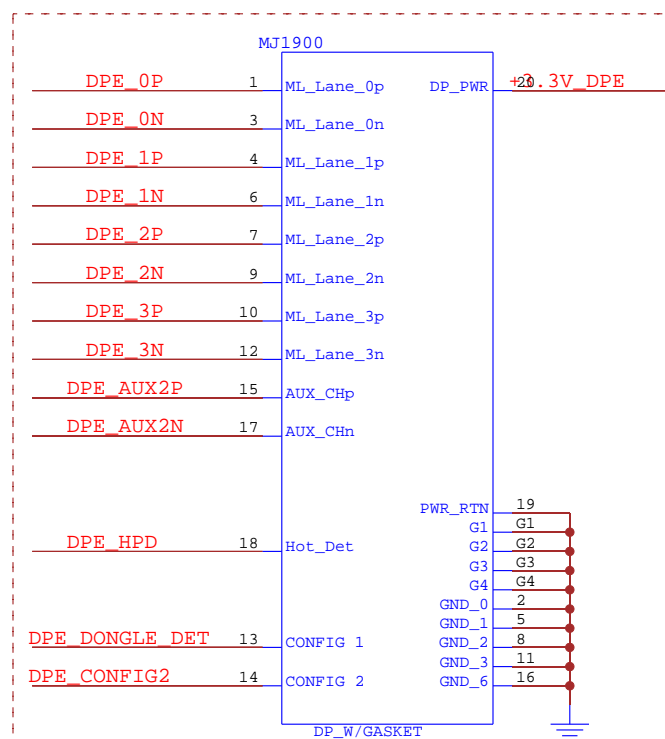
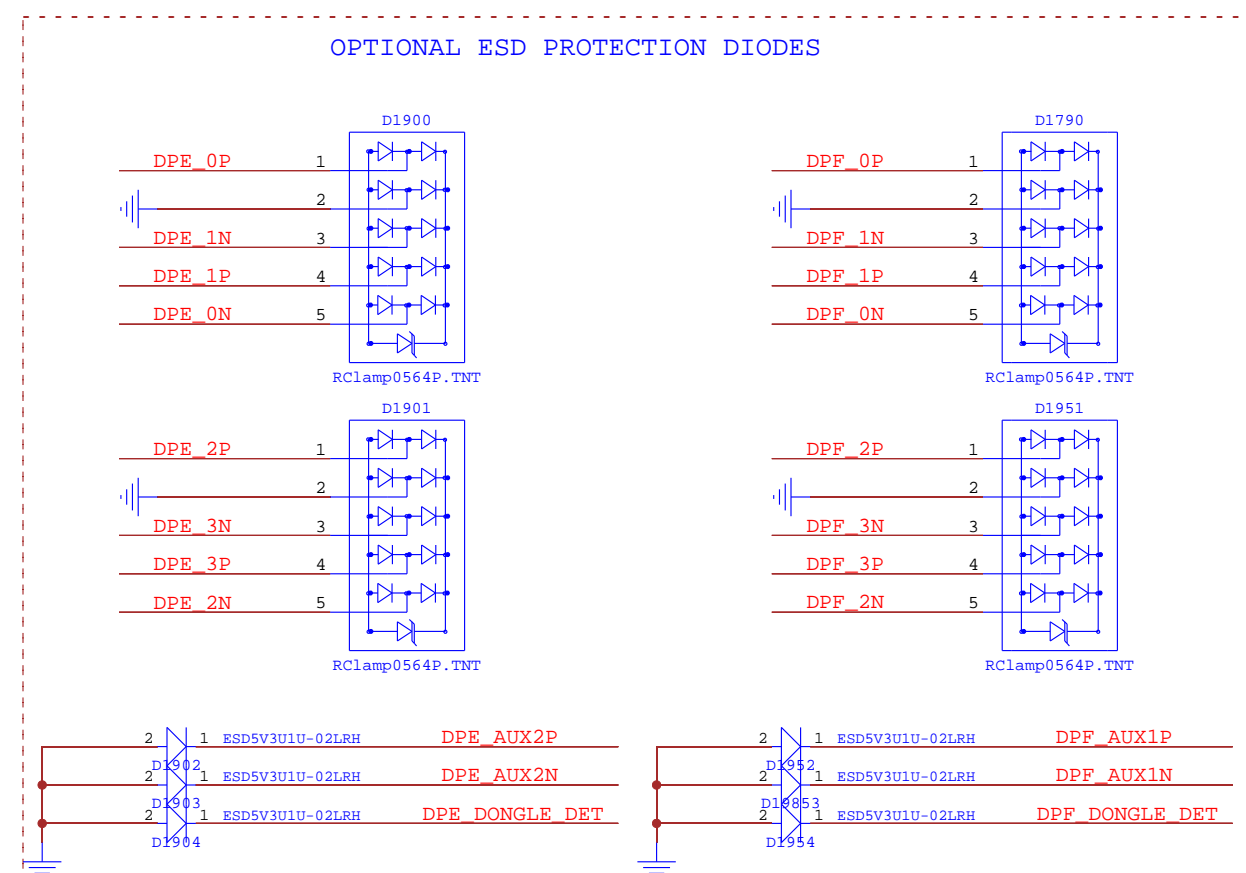
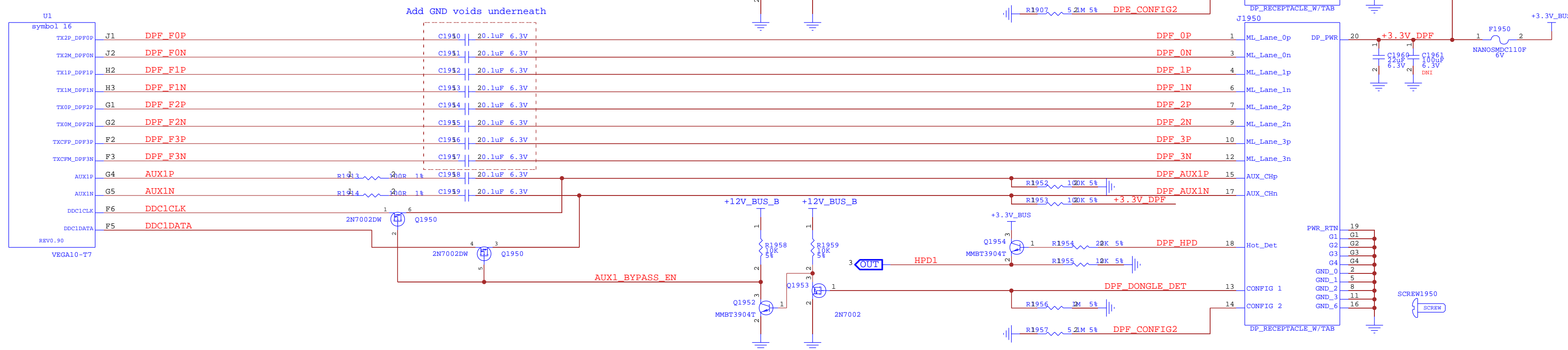
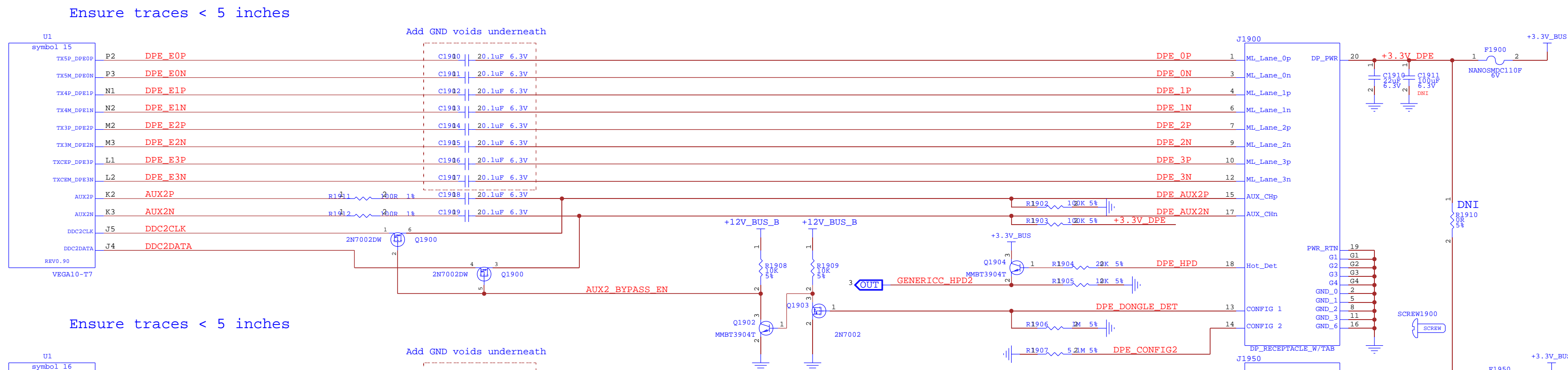
SHEET NUMBER: 5 OF 25

DOCUMENT NUMBER: 105-D05057-00

NOTES: NOTE

TITLE:

TITLE



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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Vega10 - TMDPEF 2xDP

DATE: Fri Feb 03 13:36:27 2017

SHEET NUMBER: 6 OF 25

NOTES: NOTE

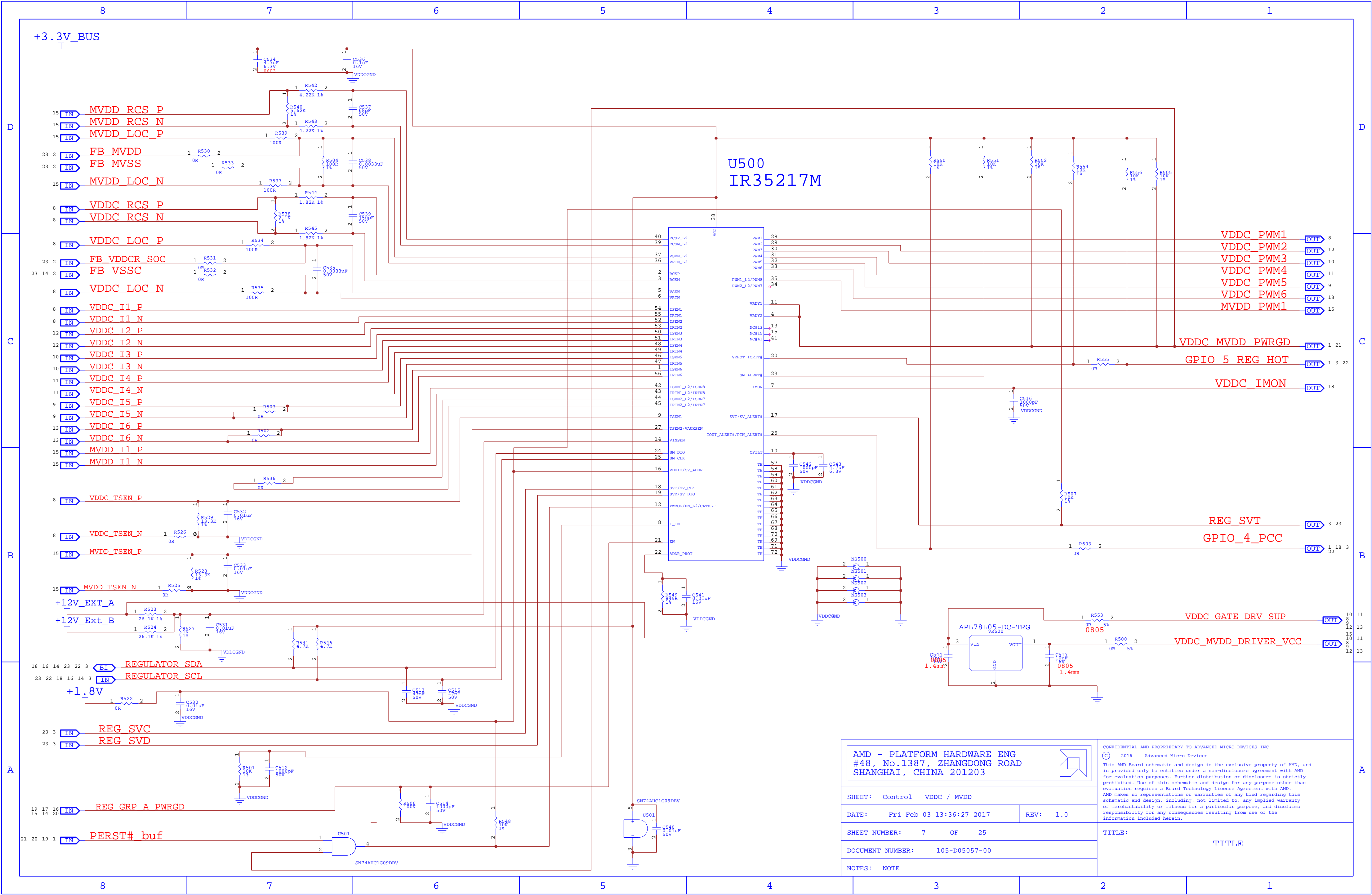
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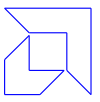
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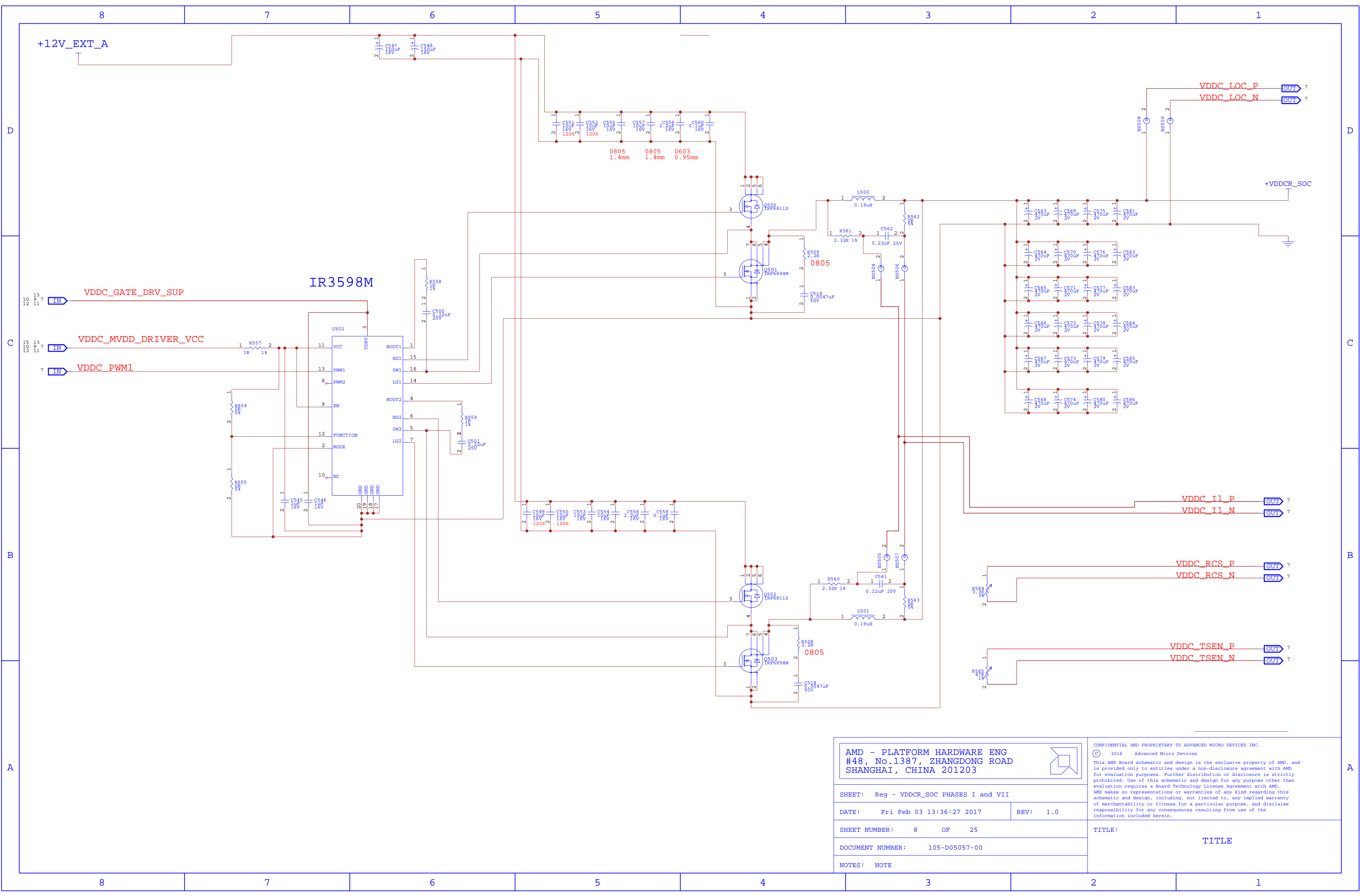
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SHEET: Control - VDDC / MVDD			<div>TITLE:</div> <div>TITLE</div>	
DATE: Fri Feb 03 13:36:27 2017		REV: 1.0		
SHEET NUMBER: 7 OF 25				
DOCUMENT NUMBER: 105-D05057-00				
NOTES: NOTE				



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#48, No.1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

SHEET: Reg - VDDCR_SOC PHASES I and VII

DATE: Fri Feb 03 13:36:27 2017

SHEET NUMBER: 8 OF 25

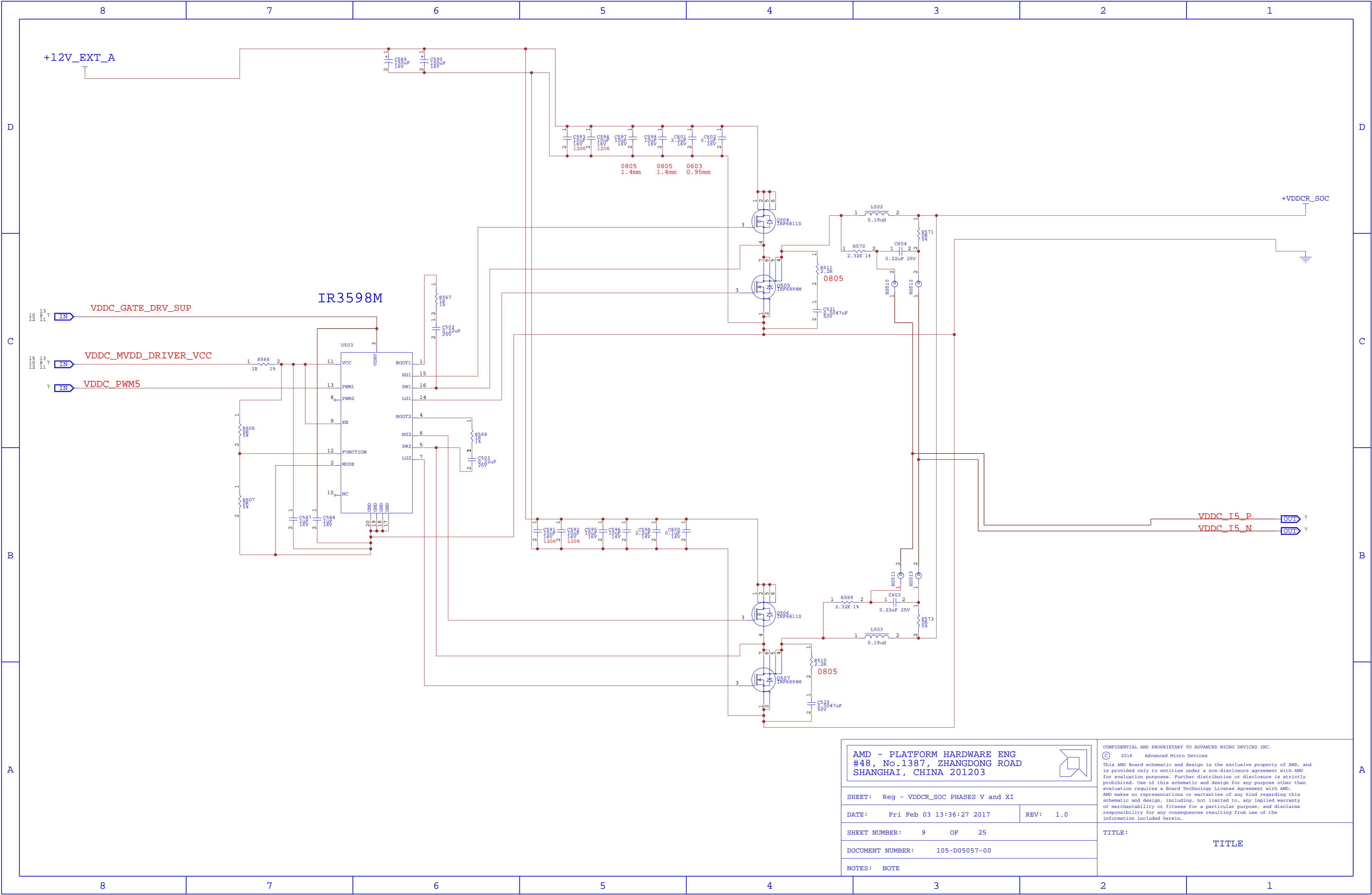
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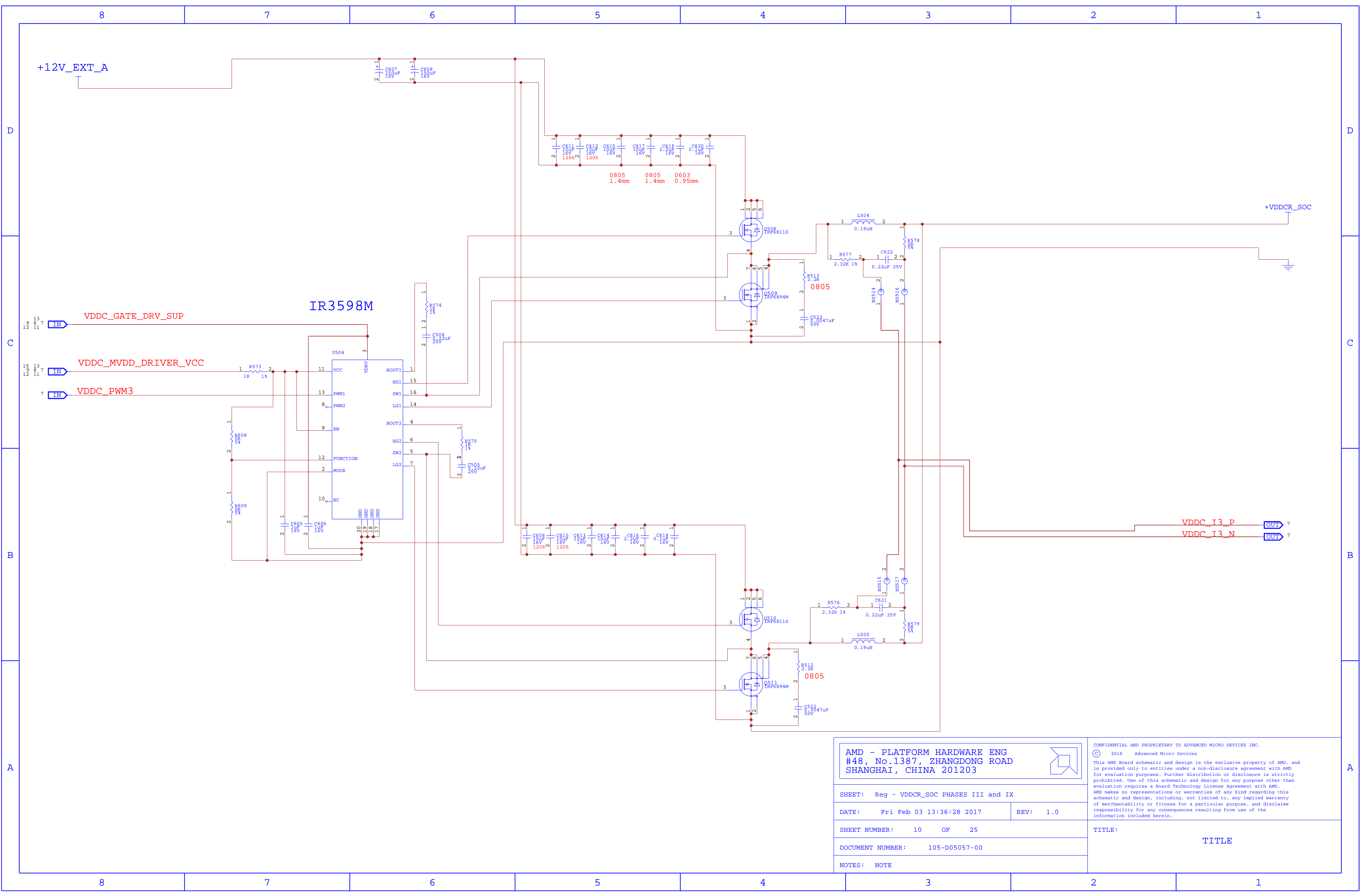
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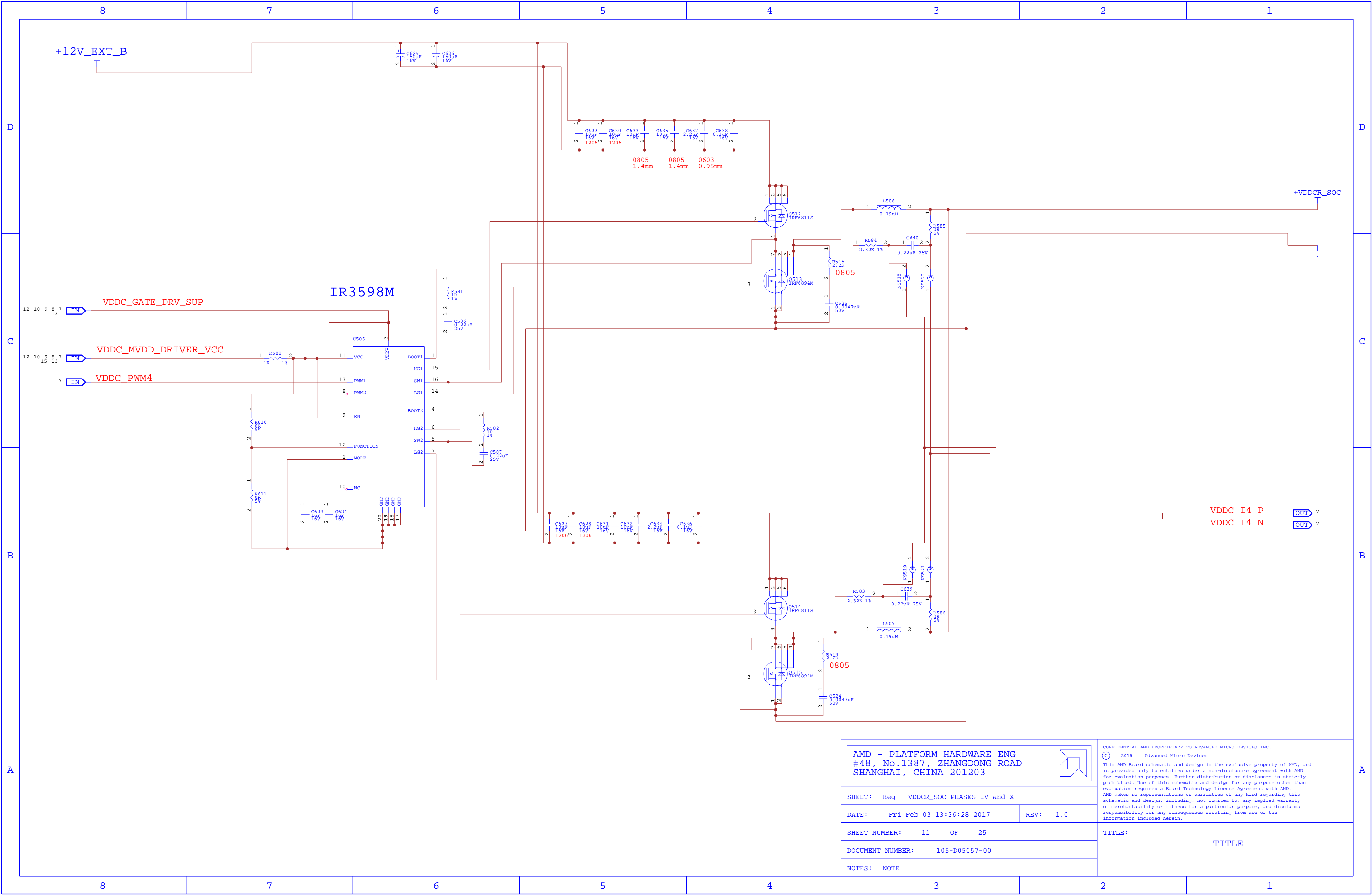
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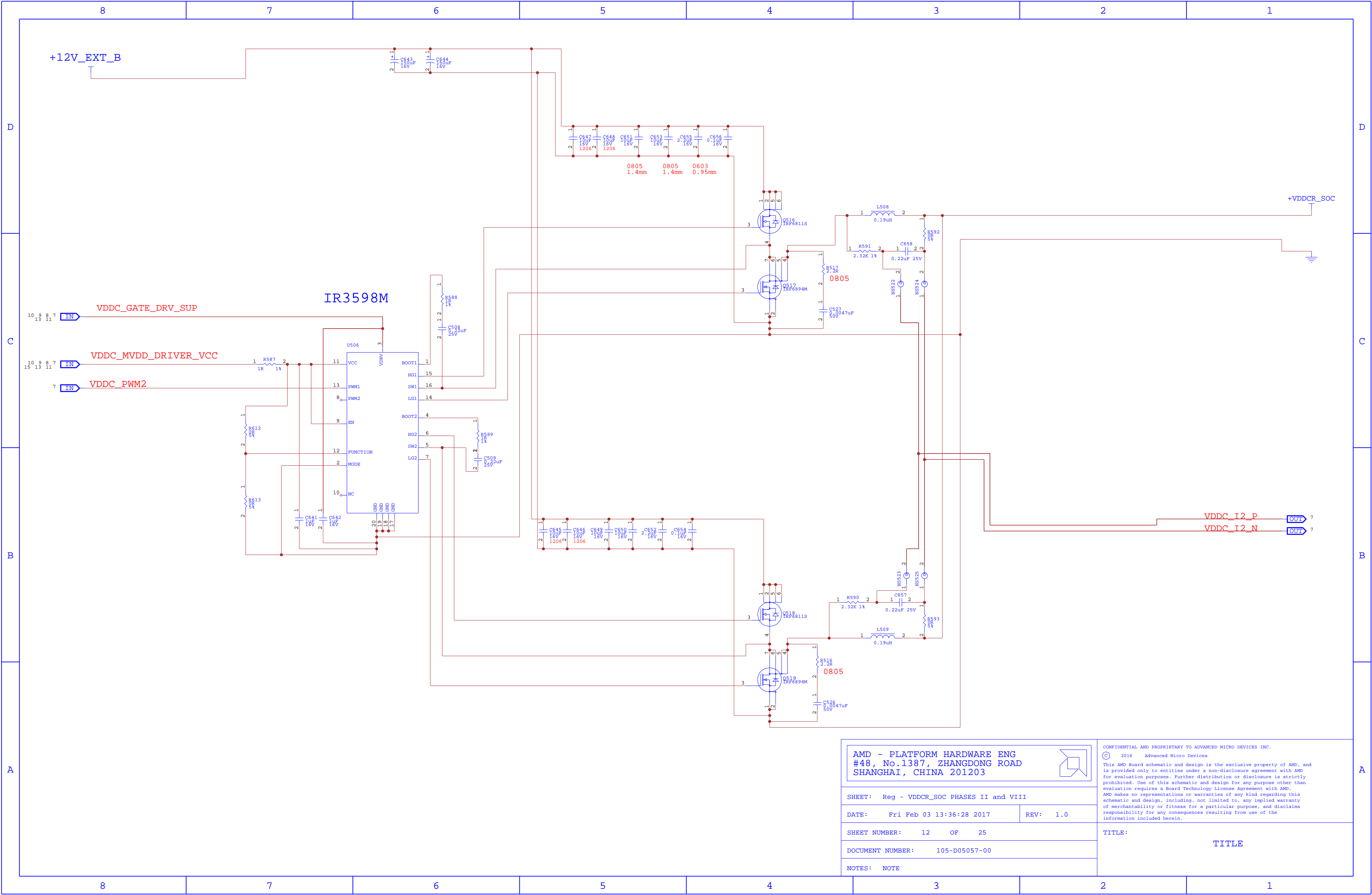
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SHEET: Reg - VDDCR_SOC PHASES V and XI			TITLE: TITLE		
DATE: Fri Feb 03 13:36:27 2017		REV: 1.0			
SHEET NUMBER: 9 OF 25					
DOCUMENT NUMBER: 105-D05057-00					
NOTES: NOTE					



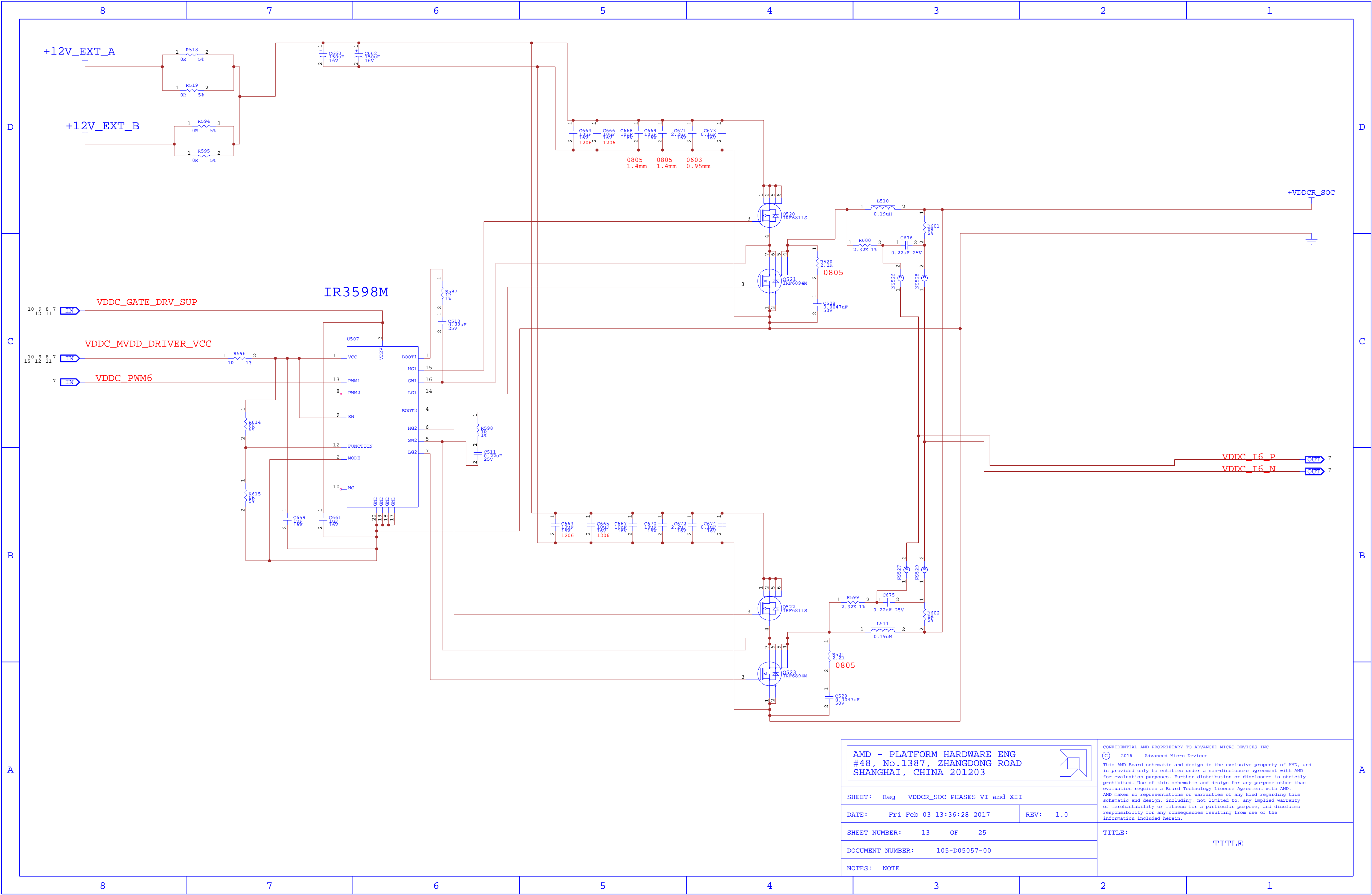
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SHEET: Reg - VDDCR_SOC PHASES III and IX			TITLE: <div>TITLE</div>		
DATE: Fri Feb 03 13:36:28 2017		REV: 1.0			
SHEET NUMBER: 10 OF 25					
DOCUMENT NUMBER: 105-D05057-00					
NOTES: NOTE					



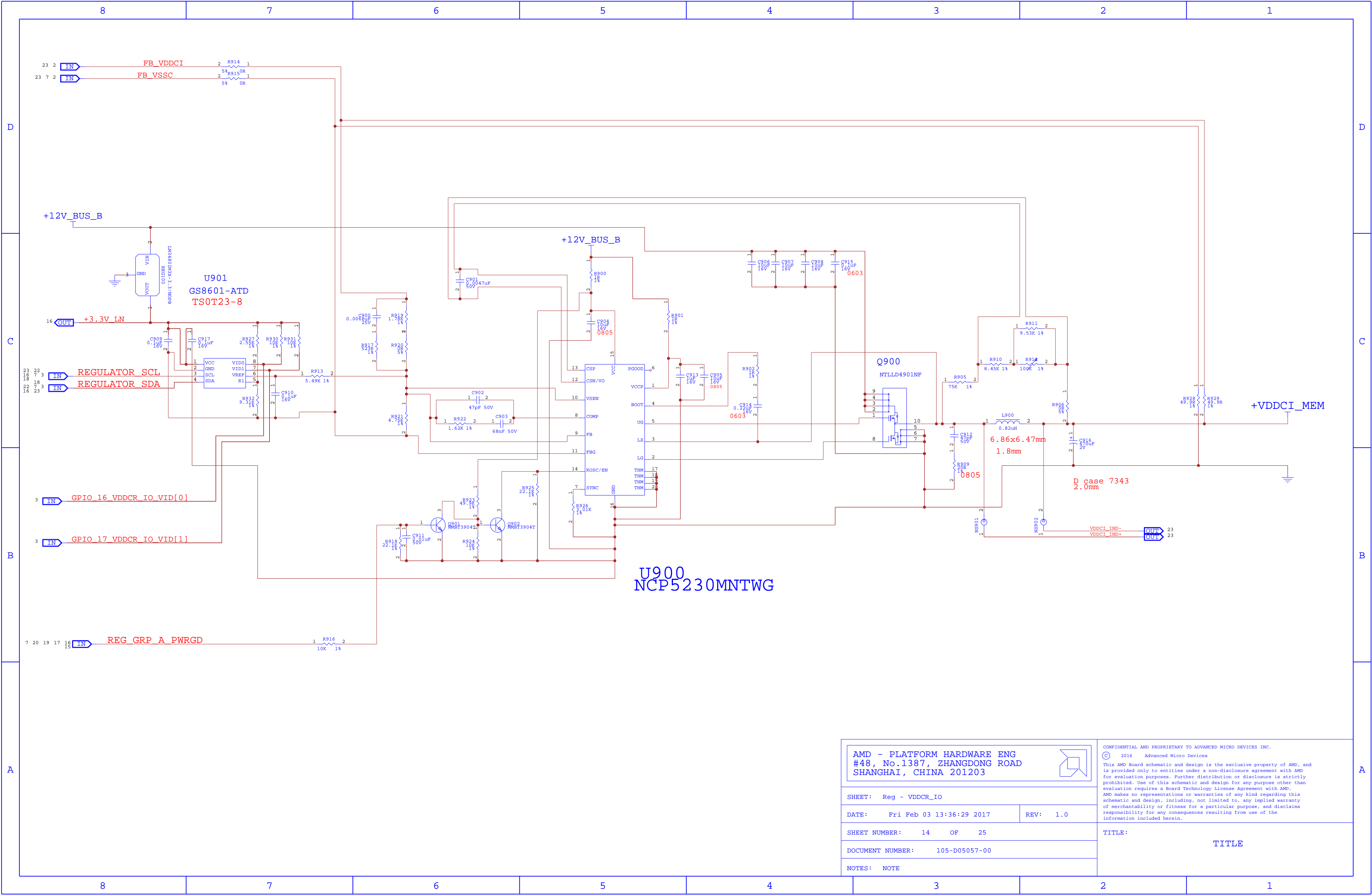
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SHEET: Reg - VDDCR_SOC PHASES IV and X		TITLE: TITLE	
DATE: Fri Feb 03 13:36:28 2017	REV: 1.0		
SHEET NUMBER: 11 OF 25			
DOCUMENT NUMBER: 105-D05057-00			
NOTES: NOTE			



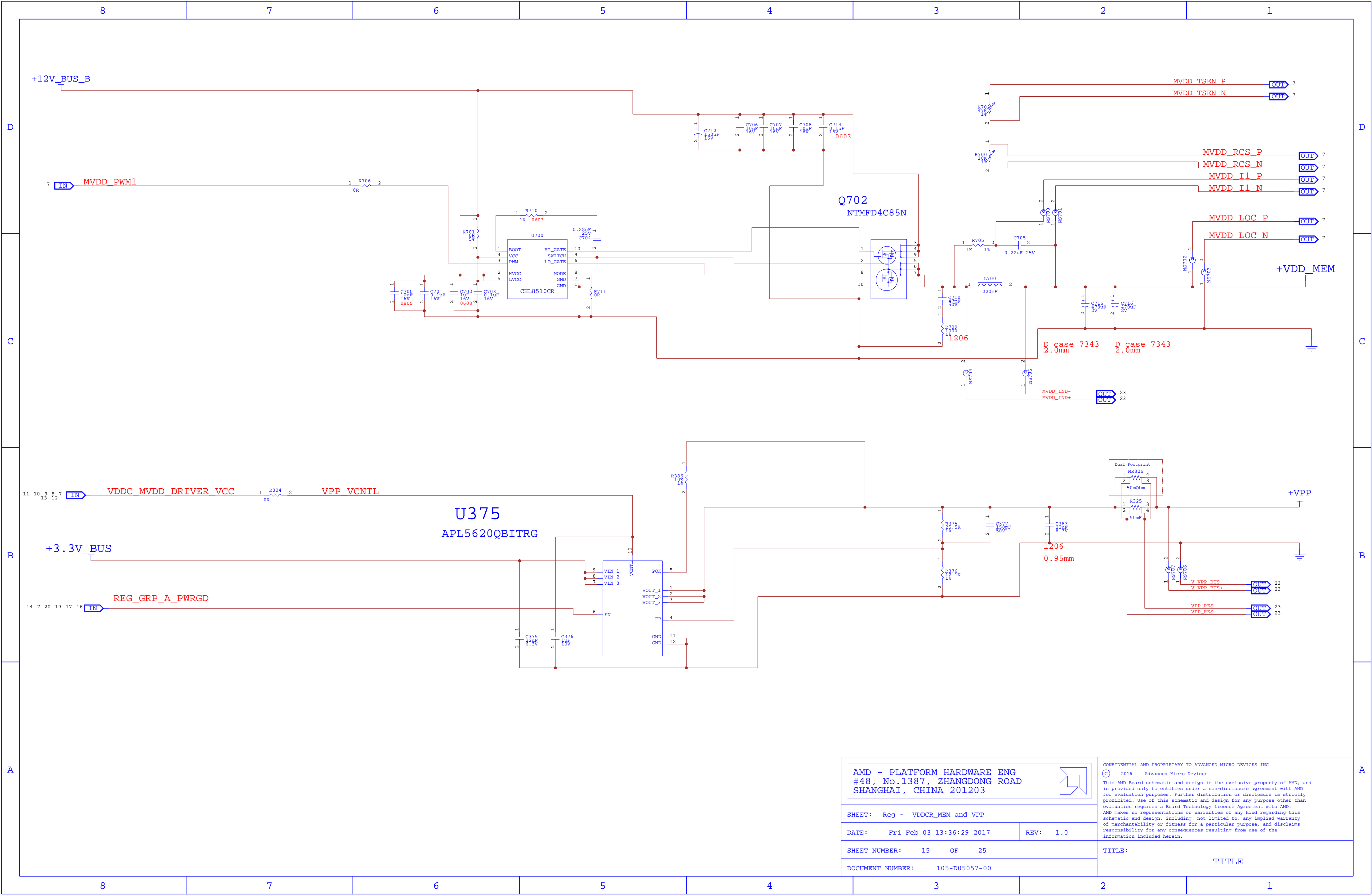
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SHEET: Reg - VDDCR_SOC PHASES II and VIII		<div>TITLE:</div> <div>TITLE</div>
DATE: Fri Feb 03 13:36:28 2017	REV: 1.0	
SHEET NUMBER: 12 OF 25		
DOCUMENT NUMBER: 105-D05057-00		
NOTES: NOTE		




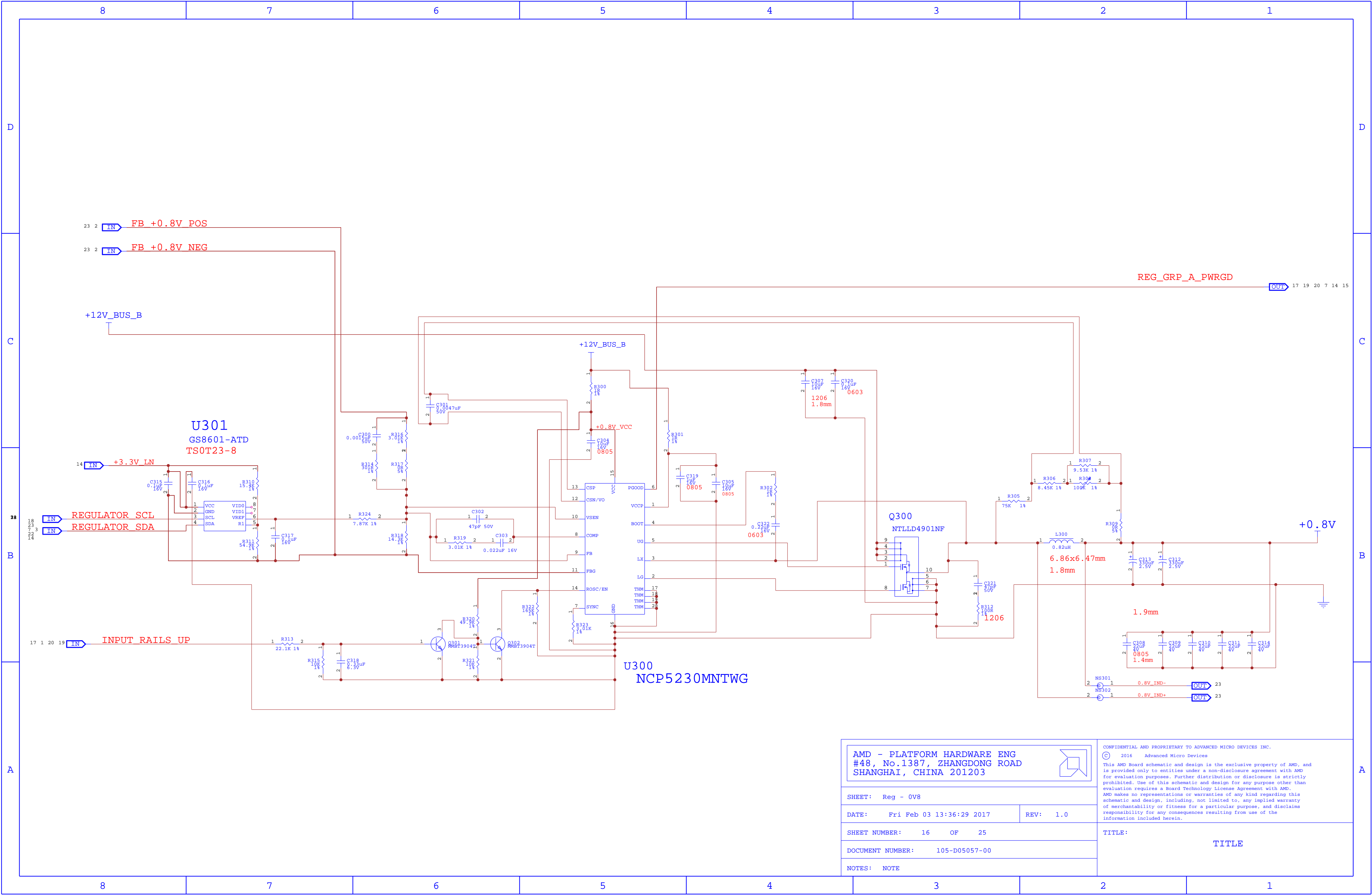
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SHEET: Reg - VDDCR_SOC PHASES VI and XII		TITLE: TITLE	
DATE: Fri Feb 03 13:36:28 2017	REV: 1.0		
SHEET NUMBER: 13 OF 25			
DOCUMENT NUMBER: 105-D05057-00			
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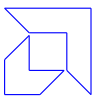


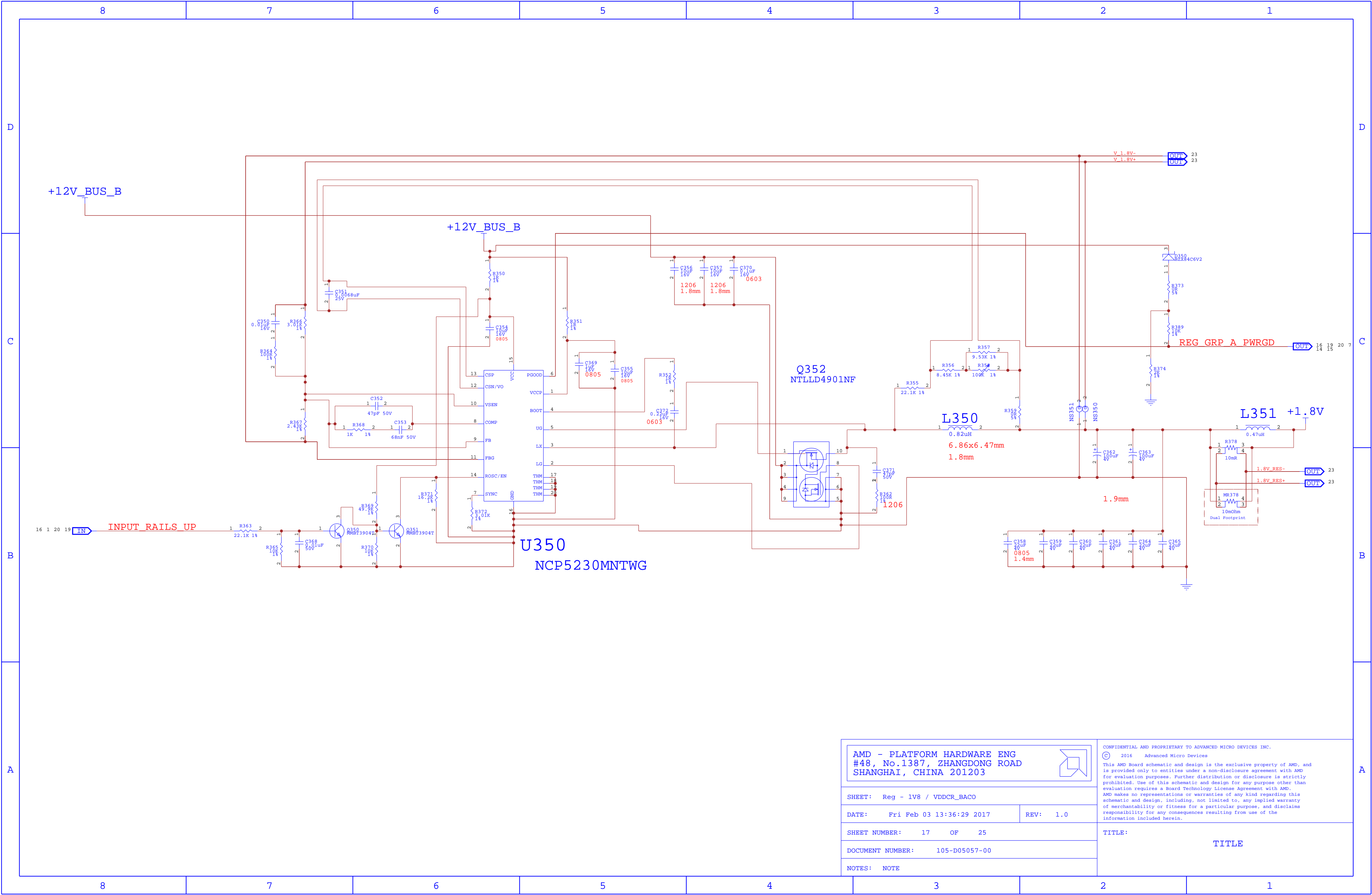
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SHEET: Reg - VDDCR_IO		TITLE: TITLE	
DATE: Fri Feb 03 13:36:29 2017	REV: 1.0		
SHEET NUMBER: 14 OF 25			
DOCUMENT NUMBER: 105-D05057-00			
NOTES: NOTE			



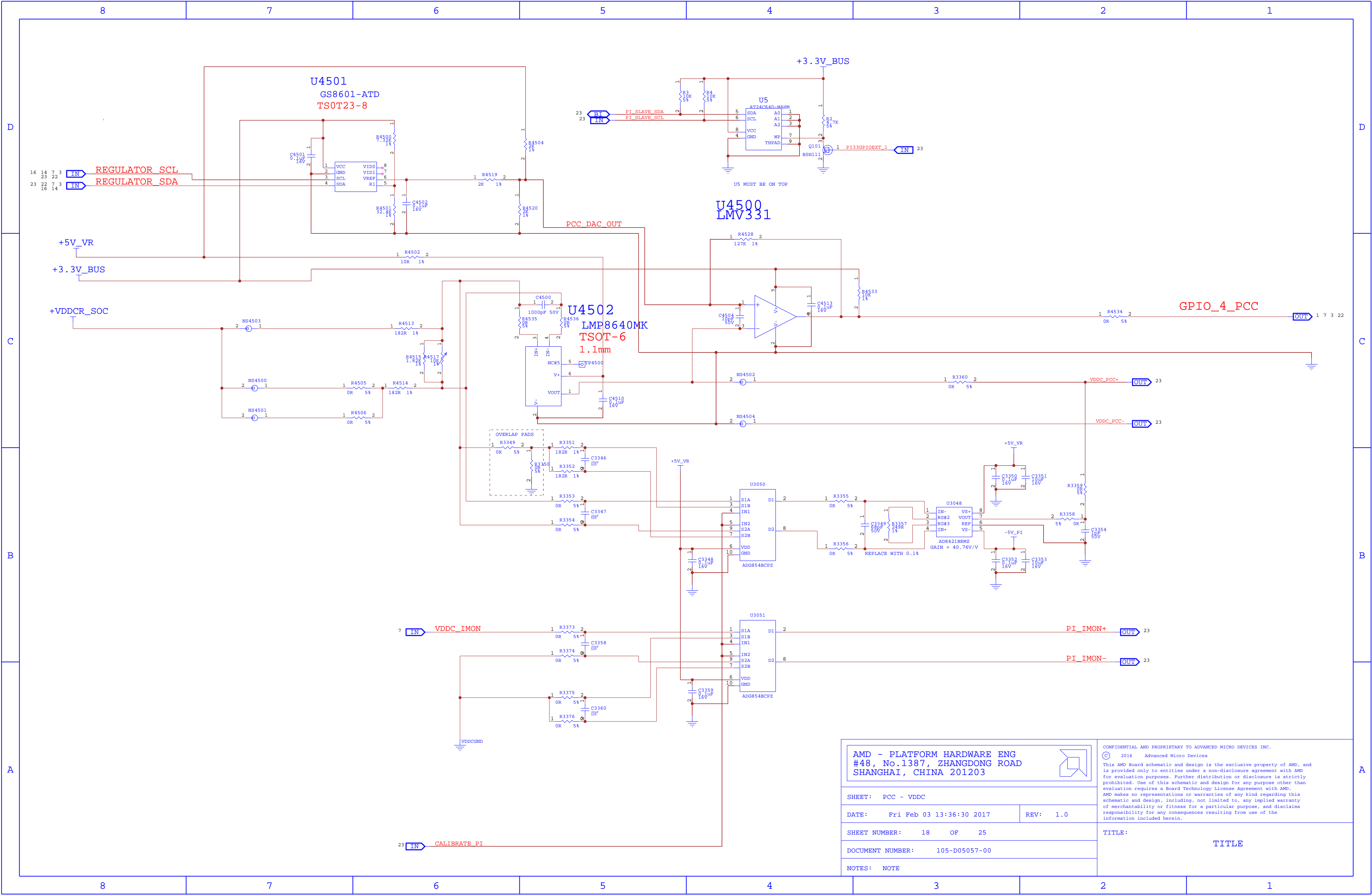
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SHEET: Reg - VDDCR_MEM and VPP			TITLE:	
DATE: Fri Feb 03 13:36:29 2017	REV: 1.0	TITLE		
SHEET NUMBER: 15 OF 25				
DOCUMENT NUMBER: 105-D05057-00				



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SHEET: Reg - 0V8				TITLE:	
DATE: Fri Feb 03 13:36:29 2017		REV: 1.0		TITLE	
SHEET NUMBER: 16 OF 25					
DOCUMENT NUMBER: 105-D05057-00					
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SHEET: Reg - 1V8 / VDDCR_BACO		TITLE: TITLE	
DATE: Fri Feb 03 13:36:29 2017	REV: 1.0		
SHEET NUMBER: 17 OF 25			
DOCUMENT NUMBER: 105-D05057-00			
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SHANGHAI, CHINA 201203

SHEET: PCC - VDDC

DATE: Fri Feb 03 13:36:30 2017

SHEET NUMBER: 18 OF 25

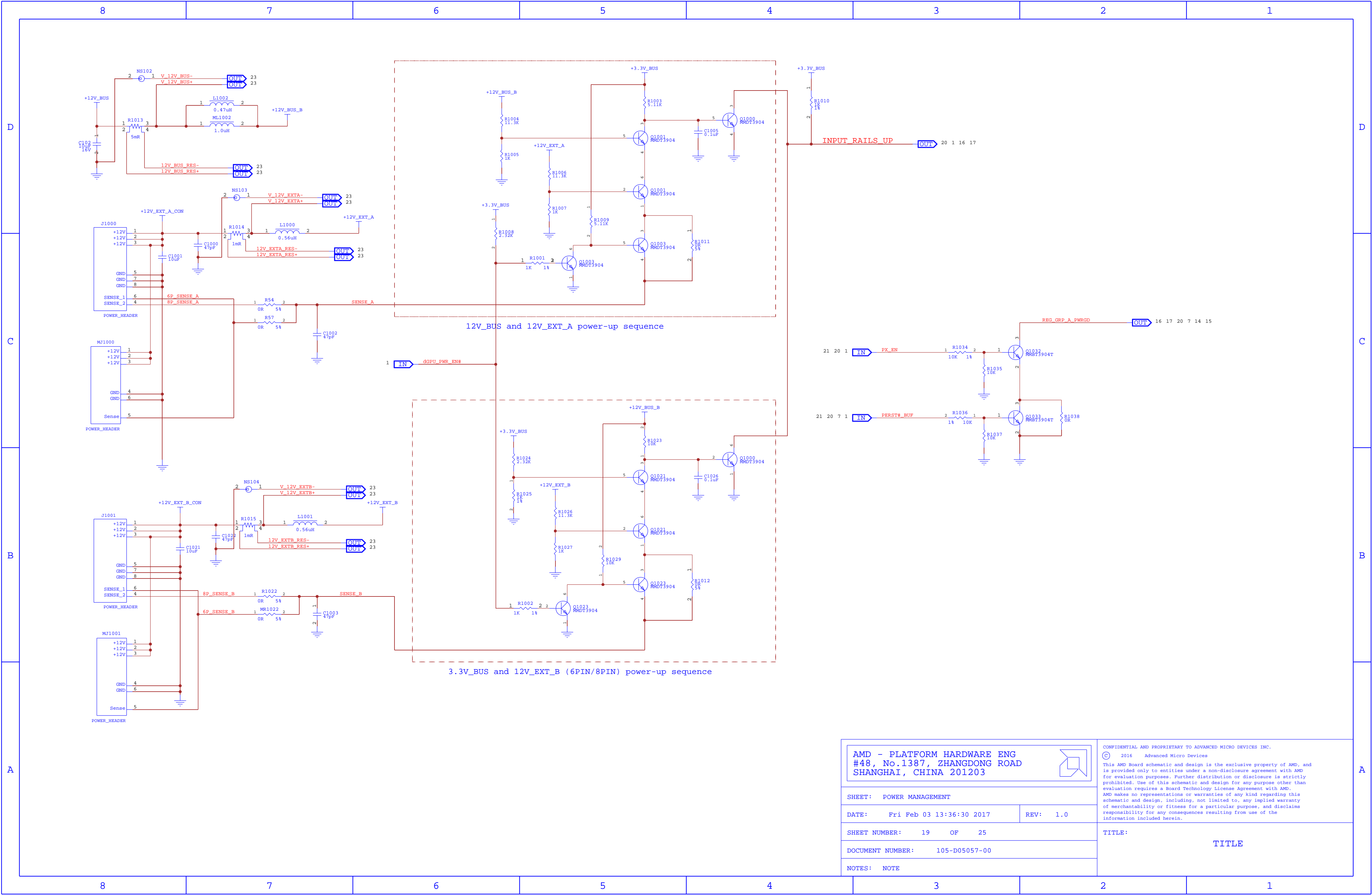
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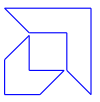
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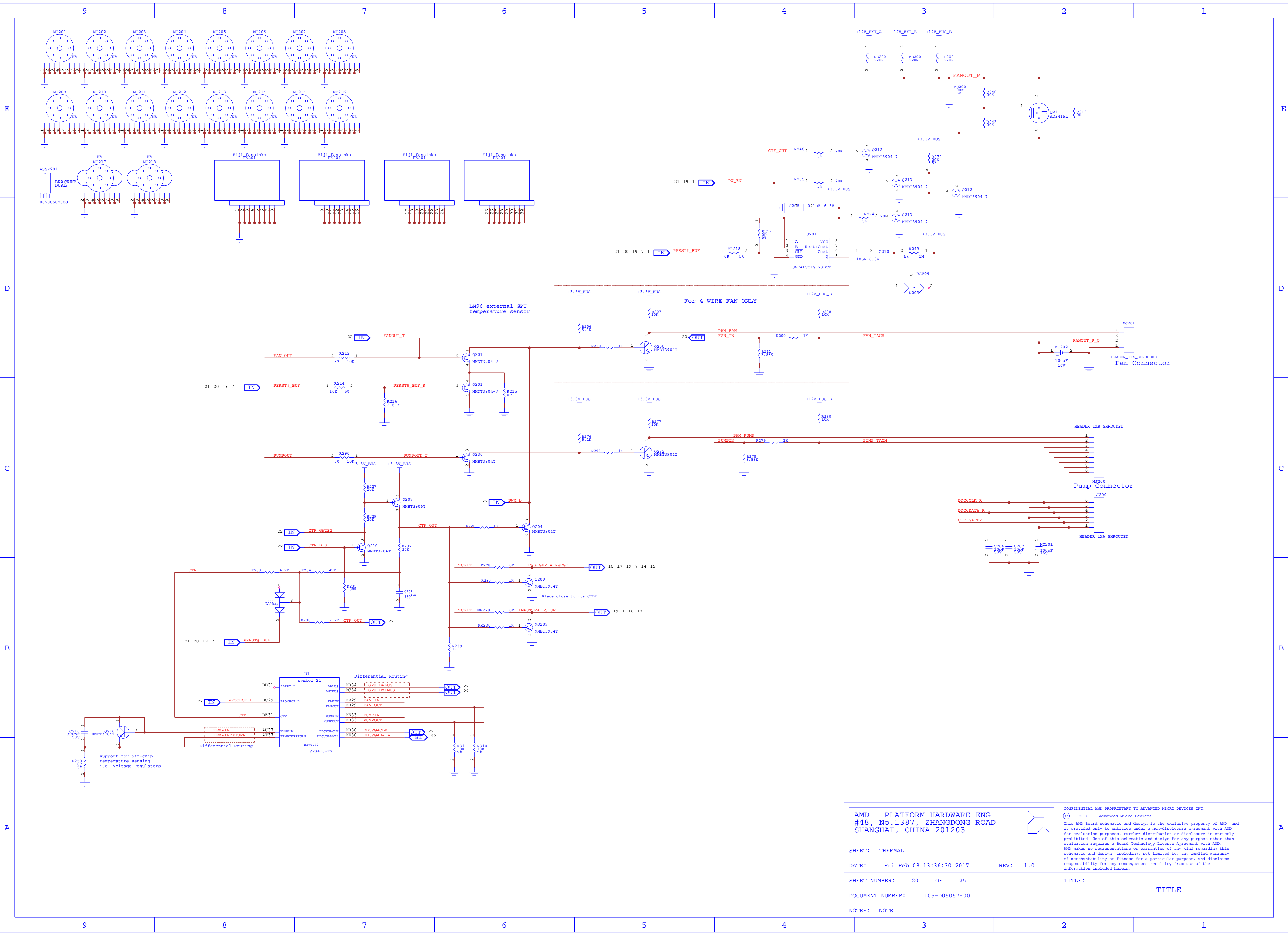
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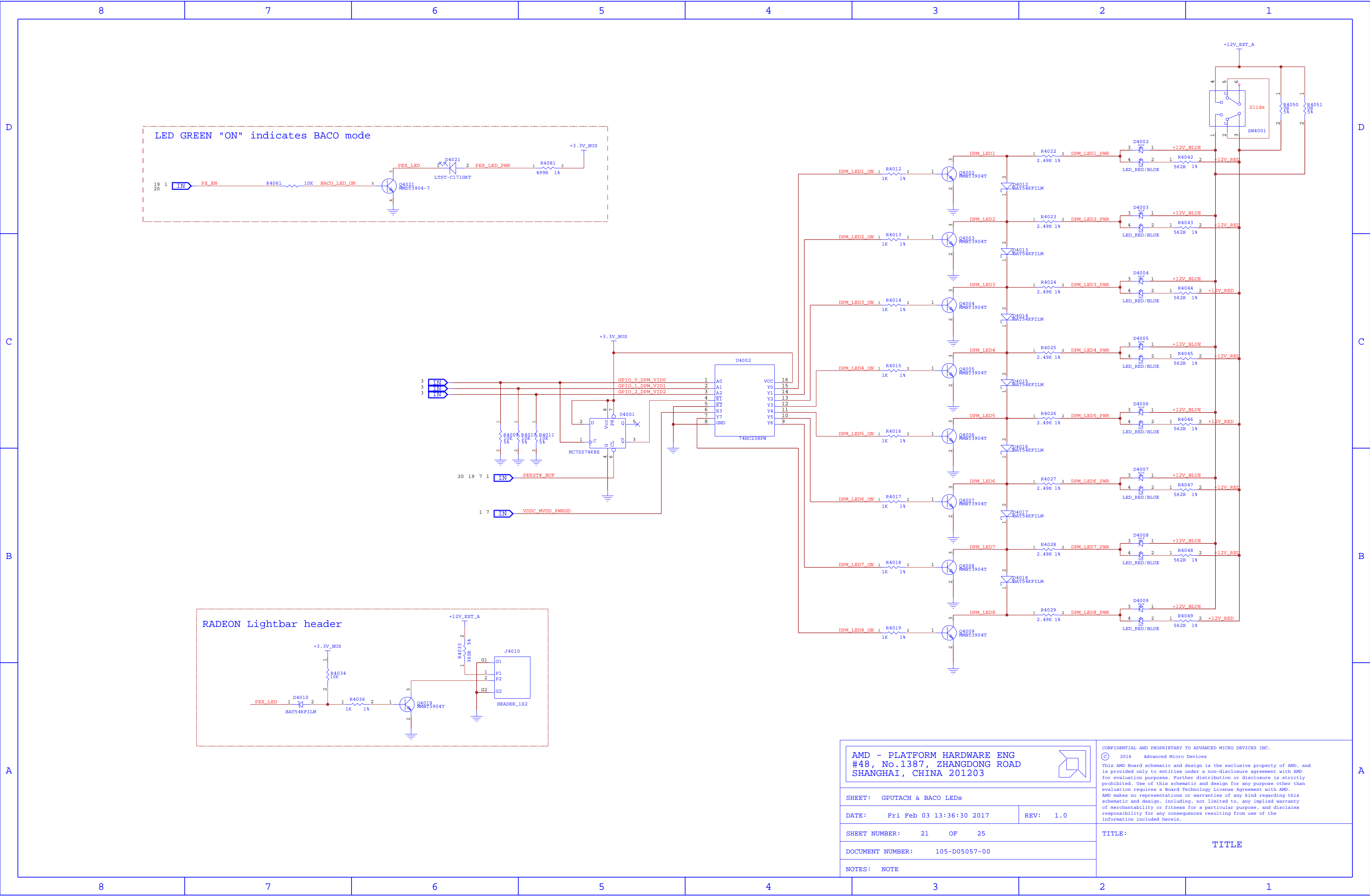
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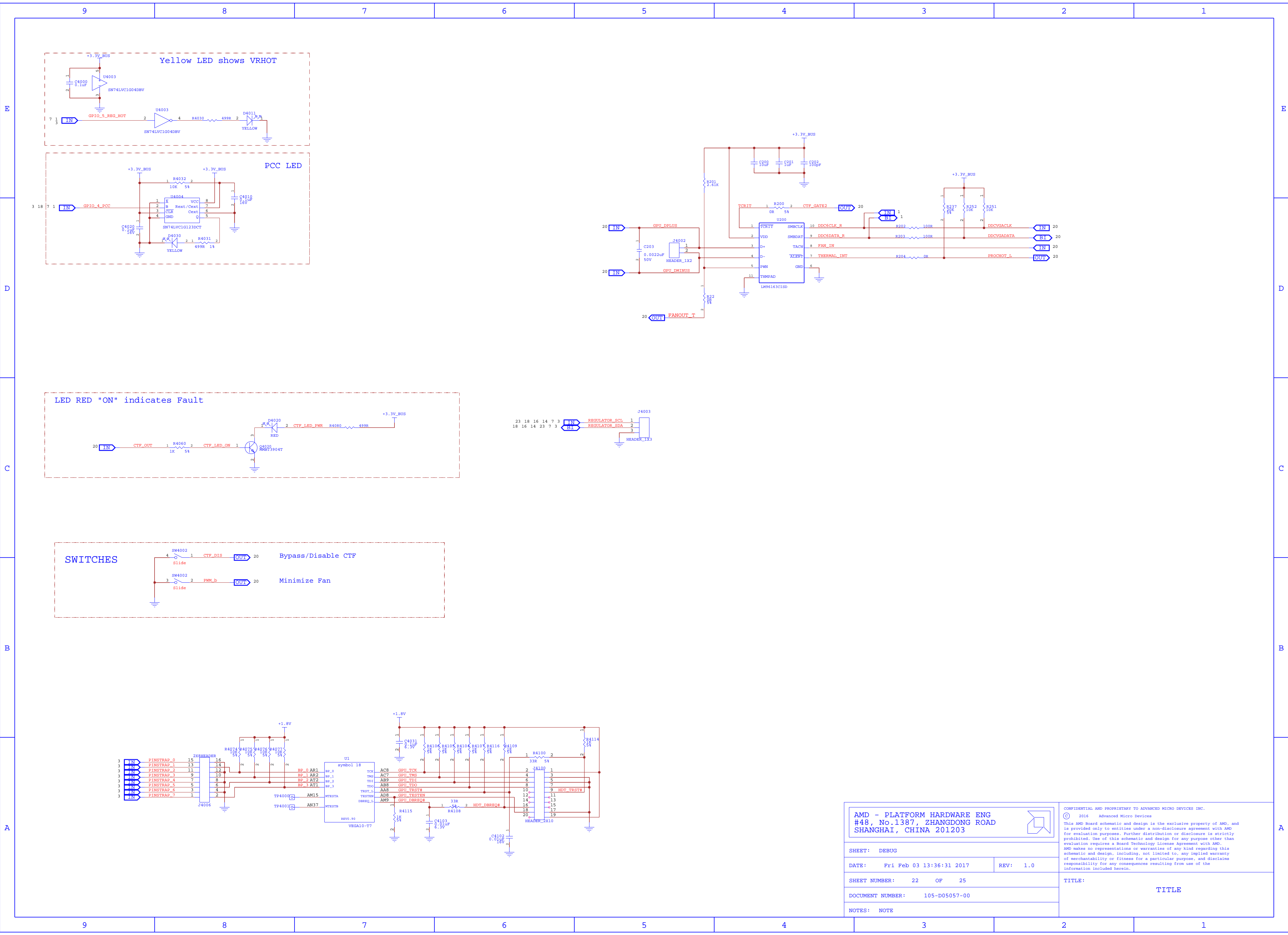
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SHEET: POWER MANAGEMENT			TITLE: TITLE	
DATE: Fri Feb 03 13:36:30 2017	REV: 1.0			
SHEET NUMBER: 19 OF 25				
DOCUMENT NUMBER: 105-D05057-00				
NOTES: NOTE				







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SHEET: DEBUG				TITLE:	
DATE: Fri Feb 03 13:36:31 2017		REV: 1.0		TITLE	
SHEET NUMBER: 22 OF 25					
DOCUMENT NUMBER: 105-D05057-00					
NOTES: NOTE					

D



B



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TITLE

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SHEET: BLOCK DIAGRAM			TITLE: TITLE		
DATE: Thu Feb 02 12:25:15 2017		REV: 1.0			
SHEET NUMBER: 24 OF 25					
DOCUMENT NUMBER: 105-D05057-00					
NOTES: NOTE					

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<div>AMD</div>				<div></div>			TITLE:						DOCUMENT NUMBER: 105-D05057-00			DATE: Fri Feb 03 11:52:28 2017			SHEET NUMBER: 25 OF 25			REV: 1.0		
REVISION HISTORY						ENGINEER: XXX			NOTES: NOTE			CONFIDENTIAL AND PROPRIETARY TO ADVANCED MICRO DEVICES INC. C • 2016 Advanced Micro Devices This AMD Board schematic and design is the exclusive property of AMD, and is provided only to entities under a non-disclosure agreement with AMD for evaluation purposes. Further distribution or disclosure is strictly prohibited. Use of this schematic and design for any purpose other than evaluation requires a Board Technology License Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, not limited to, any implied warranty of merchantability or fitness for a particular purpose, and disclaims responsibility for any consequences resulting from use of the information included herein.						AMD - PLATFORM HARDWARE ENG #48, No.1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203						
D	SCH Rev	PCB Rev	Date	REVISION DESCRIPTON																	D			
	0	A	10/9/15	Initial schematic creation																				
		B	6/30/16	Many Changes on PI circuit , Minor Chnages on SMPS																				
		C	9/30/16	Many Changes on PI circuit , ASIC SYMBOL UPDATED FOR FLASH ROM INTERFACE , flash ROM SI/SO swapped , RP1 added																				
		D	11/29/16	Changes on PI circuit , 100MHz HCSL clock source replced (contact AMD for detailes)																				
		E	01/05/17	PI circuit removed , 200R added to DP AUX (6 resistors)																				
		-00	02/02/17	1.8V/VPP Kelvin resistors dual footprinted , DP AUX (6 resistors changed to 100R) , Changed R4033 to 360R 1206 and moved to 12V_AUX , SMBUS Address note swap , J4001 removed , R115/R116 changed to 61.9R , R205 added																				
C																					C			
B																					B			
A																					A			
8				7			6			5			4			3			2			1		